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# Asymmetrical Single Phase Reduced Switch Nine Level Inverter with Trinary Sequence DC Input for PV based Renewable Energy Systems

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**A B S T R A C T**

This paper presents an innovative Asymmetrical Single-Phase Nine Level Inverter (ASRNLI) that stands out among various available configurations. The design achieves a staircase-like voltage pattern with the highest number of levels while utilizing a reduced number of components. Compared to conventional systems, asymmetric multilevel inverters require fewer components yet manage to create a cascade structure with multiple output levels. The ASRNLI configuration consists of two independent DC sources and 10 switches, allowing it to generate any desired level. This setup offers several advantages, including improved output voltage quality attributed to the switches' low blocking voltage. It proves particularly valuable in scenarios where asymmetric DC voltage sources are accessible, such as in modern electric vehicles and AC mini-grids powered by renewable energy sources. To generate gate pulses, the ASRNLI employs the level-shifted pulse width modulation approach. Validation of the suggested ASRNLI configuration was carried out through both MATLAB simulations and the construction of a prototype. The output waveform demonstrated a Total Harmonic Distortion (THD) of 13.50% at the highest fundamental voltage of 400V. Throughout this article, the effectiveness of the ASRNLI configuration is supported by findings from simulations and experimental tests, showcasing its potential as a promising solution for practical applications.

## 1. Introduction

Multilevel inverters (MLIs) have emerged as a prominent option for integrating renewable energy sources. They offer a superior solution for power system requirements that necessitate a high-quality voltage profile. Over the recent years, numerous scholars have introduced innovative MLI configurations. These advancements focus on minimizing the need for non-essential components such as switches, gate drivers, and auxiliary power supplies, while enhancing overall performance.

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Arun et al. [1] proposed a parallel-linked NPC-PWM inverter for motor transmission, and various modulation techniques are examined to identify the optimal modulation approach. Arun et al. [2] described a brand-new PWM technique for removing common-mode voltage in odd multilevel inverters that is built on the three zero common-mode vector principles. This PWM method can be represented similarly to traditional PWM in multilevel inverters and can be accurately depicted in an active two-level voltage converter. The main objective is to improve efficiency by combining cells with different characteristics, but this is limited by the need for separate supplies for each cell is presented by Arun et al. [3]. To address this issue, several three-phase inverter designs have been used as high-voltage cells. The study compares cascaded H-Bridge inverters and multiple circuits with diode-clamped inverters, as well as mitigation techniques such as SPWM. Vijayakumar et al. [4] presented the primary benefit of the CHB topology is the high accuracy output voltage achieved by raising the number of voltage levels. For CHB constructions, it is essential to use numerous independent DC voltage sources. Both controllers are modified in accordance with the dynamic behaviour of the proposed model for each ACHMI in the N-series H-bridge converter at each output interface. Each ACHMI is given a unique number. A thorough analysis of the various PWM techniques will be provided, along with an assessment of their benefits and drawbacks and a foundation for choosing the best technique Total harmonic distortion (THD) over the full linear modulation index range, voltage and current patterns, and spectra are used as the general figures of merit to evaluate the PWM techniques are presented by Arun et al. [5]. In addition, a novel open-switch fault-diagnostic technique for an N-level cascaded H-bridge multilevel inverter is presented by Sébastien [6] in this article, which makes use of half-cycle bridge voltages as fault-identifying traits. For cascaded inverters with different voltage levels, this quick detection technique can spot the faulty switch within one fundamental output voltage interval. Venkataramanaiah et al.[7] developed a single-phase multilevel inverter with enhanced output voltage quality with asymmetrically regulated DC-link voltages by lowering total harmonic distortion (THD) and filter size. For uneven numerous inverter setups, hybrid inverters are favoured because of their higher effectiveness. Kamaldeep Boora and Jagdish Kumar [8] discussed multilevel inverters (MLIs) are widely used in high-power applications. Tiago et al. [9] presented MLIs are mostly used in high-voltage applications due to their numerous benefits, which include improved power quality, reduced voltage stress across power switches, conformance with electromagnetic fields, and smaller component sizes. Various H-bridge based cascaded MLI configurations have been proposed by Vafakhah et al. [10]and Grandi et al. [11] with different approaches to determine the size of the sources. These inverters employ a wide range of DC source voltage magnitudes to synthesize the desired output level is presented by Arash et al. [12] and Anilkumar et al [13]. Arun et al. [14] developed a cascaded MLI utilizes series connections of elementary units to generate positive output levels and adds an H-bridge for voltage generation in both cycles. Although this design consists of various voltage sources and power switches, it requires a high number of DC sources for low-level MLIs.

Vijayakumar et al. [15] developed an asymmetrical MLI with an E-type module is presented, aiming to reduce components and generate output in both cycles without the need for an H-bridge. However, this MLI can only operate with asymmetric binary DC link voltage. Babaei et al [16]-[18] introduces a new basic unit for cascaded MLI, but the quantity of input sources, IGBTs, and drivers in this unit is high. Samadaei et al. [19] and Alishah et al. [20] presented a new hybrid symmetric and asymmetric cascaded MLIs, but these topologies also require a higher number of input voltage sources in their basic units. Gautam [21] and Boora and Kumar in [22] developed MLIs with fewer components have been designed, but to achieve the desired output voltage levels, a variety of DC sources are still needed. The trinary DC source MLI is presented by Majumdar et al. [23] with 10 switches and 2 input sources. However, this proposed MLI requires an H-bridge unit to generate negative voltage levels, and the switching elements of the output H-bridge are under significant voltage stress, which is a notable drawback of the topology. Bana et al. [24], Zeng et al. [25] and Prabaharan et al. [26] proposed a modified MLI configurations with reduced components, but these topologies also rely on a large number of DC sources to generate the desired voltage output levels. However, the majority of the previously listed setups suffer from an array of major issues are presented by Salem et al. [27] and Mondol et al. [28]. The overabundance of switching devices, Total Standing Voltage (TSV) issues, an excess of DC voltage sources and capacitors, a requirement for a supplementary polarity creating a circuit, high voltage rating of the switches, and an enormous number of high-frequency switching shifts during working all contribute to higher losses. To overcome these constraints, this work proposes an ASRNLI configuration that seeks to alleviate these difficulties. In this study, level-shifted PWM

(LSPWM) is employed, and MATLAB SIMULINK is used for the modelling tests.

The suggested configuration exhibits several key characteristics as follows:

- To achieve the highest output voltage levels, the design employs a minimal number of power electronic components, specifically reducing switches and DC sources.
- With fewer switches involved, a straightforward modulation approach effectively governs the ASRNLI setup.
- Additionally, each mode of operation entails a maximum of three switches conducting, leading to reduced switching transitions and lower conduction losses, resulting in higher overall efficiency.
- Despite utilizing only two non-identical DC sources, the configuration manages to generate a 9-level voltage output by skilfully integrating these two voltage sources.
- Notably, it incorporates a built-in capability to produce negative voltage levels without necessitating a separate H-bridge arrangement, thereby reducing Total Standing Voltage (TSV).

## 2. ASRNLI Circuit Topology

The circuitry required for the ASRNLI modular design is Shown in Figure.1. It has nine switches, eight of which are linear and one of which is reversible, as well as two DC sources. Every unidirectional switch is an IGBT that is linked to an antiparallel diode. (Current flow is reversible and unidirectional for voltage).The circuit being used contains nine switches, but only a maximum of four will be utilized to generate the intended output. This will result in minimal losses and a straightforward movement process. Additionally, the circuit will obtain some of the required DC voltage from two separate sources.

The switch that can operate in two directions, for both voltage and current, is made up of two unidirectional switches. The third configuration, with a V2/V1 number of 3, is used to locate the DC sources. A nine-level outcome is produced by this combo, with four positive, negative and one zero level. Without the use of an H-bridge circuit, this topology's primary characteristic is its capacity to generate various voltage values for negative and positive phases. The switches wiring prevents the anti-parallel diodes from moving from biased presented by Akbari et al. [29], which might lead to the sources being short-circuited. If the switches in (S1, S2, S3), (S3, S5, S6), (S4, S5, S7), (S3, S4, S6, S7), and (S7, S8, S9) are simultaneously turned ON, the DC sources will short circuit. Figure.2 shows various switching states are used to produce positive values.

To prevent this, the ASRNLI topology carefully selects the switching state to minimize the inactive band, considering all conditions. Pal et al. [30] presented an idea to cut the expense of the switch, the total standing voltage (TSV) for each level and the specific voltage stress of each switch. The unbalanced MLI architecture causes the TSV to be impacted by the voltage of the same level. The MLI's numerous switching states exhibit different positive and negative voltage levels. Switches are only activated once or twice during a half cycle. As a result, it lowers the module's switching losses for the low-level frequency PWM technique used in this research. The two major factors to consider when selecting switches for low-frequency MLI are the limiting voltage and the ability to control current in the ON state. The maximum voltage for each switch is managed by the tiered structure.

To comprehensively assess the advantages and drawbacks of the proposed structure, a comparative analysis is conducted between the recommended configuration and other recently developed MLI setups documented in existing literature. This comparison takes into account various factors, such as the number of DC voltage sources, switches, drivers, diodes, capacitors, and polarity generation.

Among the mentioned configurations, the proposed N9LI design stands out as the top performer in all aspects of comparison. When contrasted with other MLI configurations, the suggested N9LI demonstrates significant benefits in terms of reducing the required number of DC sources and components, leading to space-saving advantages and cost reduction in installation. Additionally, a noteworthy feature is its capability to generate negative voltage levels without the need for any additional circuitry.

This advantageous ability, combined with lower stress on components and devices, showcases the effective functionality of the suggested inverter compared to other existing topologies in the literature.

It is essential to highlight that while a few MLI configurations in the literature require a similar number of sources and switches, those setups rely on separate H-bridge arrangements to achieve both positive and negative voltage levels.

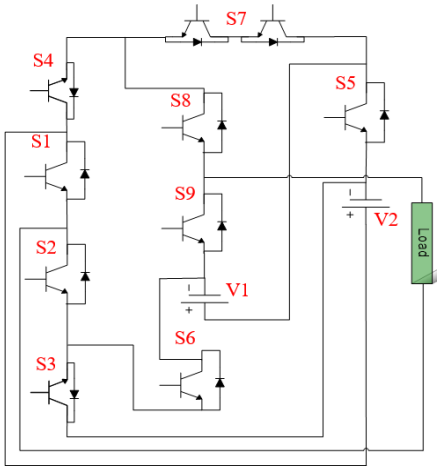
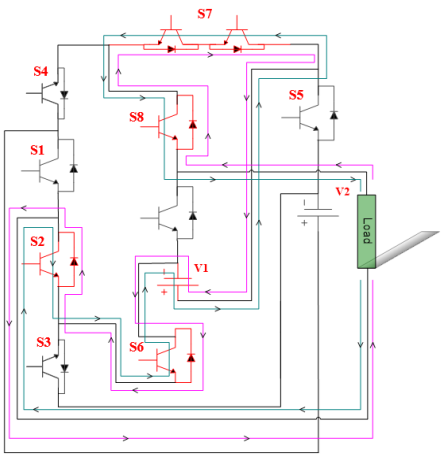


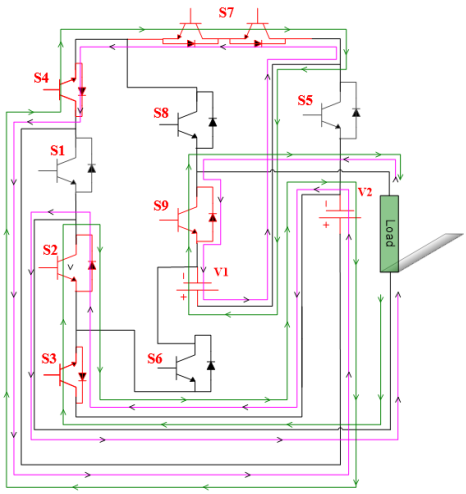

Figure. 1 shows the ASRNLI circuit diagram.

Table 1. Switching states

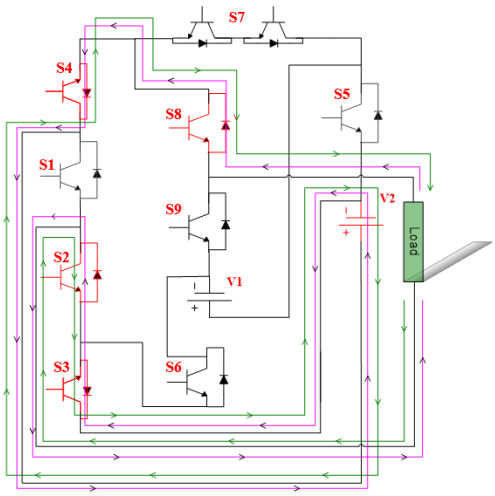
| State | Switches | | | | | | | | | O/P |
|---|---|---|---|---|---|---|---|---|---|---|
| | OFF ON | | | | | | | | | |
| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | Vdc |
| 1 | | | | | | | | | | 1 |
| 2 | | | | | | | | | | 2 |
| 3 | | | | | | | | | | 3 |
| 4 | | | | | | | | | | 4 |
| 5 | | | | | | | | | | 0 |
| 6 | | | | | | | | | | -1 |
| 7 | | | | | | | | | | -2 |
| 8 | | | | | | | | | | -3 |
| 9 | | | | | | | | | | -4 |



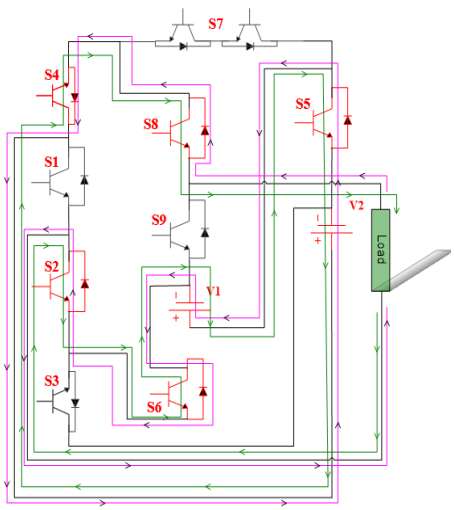

(a) Vdc



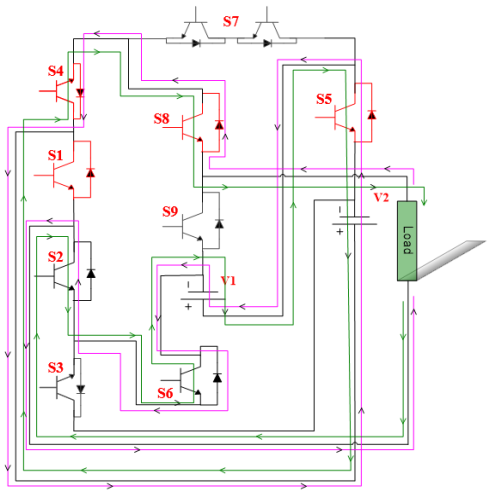

(b) 2Vdc




(c) 3Vdc




(d) 4Vdc




(e) 0 Vdc

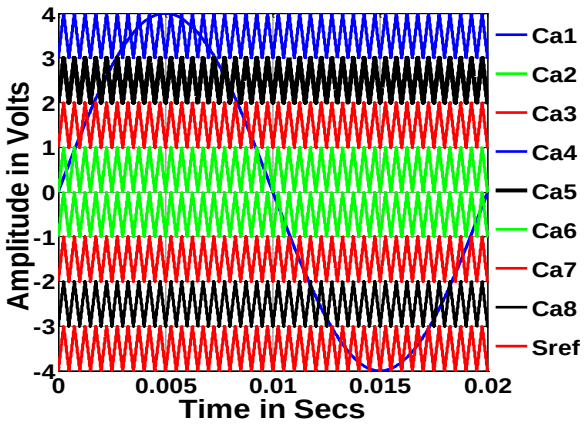
Figure.2. Various switching states are used to produce positive values.

## 3. Level Shifted PD PWM

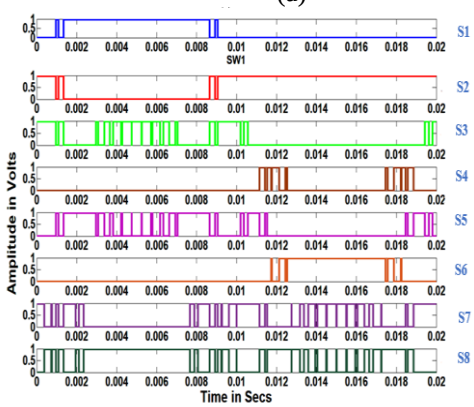
For a K-level inverter in an LSPWM approach, a similar frequency and peak-to-peak magnitude (K-1) carriers were used. Due to its ease of implementation, clear conceptualization implications, and adaptable control degrees, LS-PDPWM modulation is well-suited to become widespread in MLIs. In this case, a voltage output with nine distinct steps is generated using eight carrier signals. Carrier frequencies and peak-to-peak amplitudes are standardized across all occupied frequency bands. This configuration of carriers is known as the "phase disposition PWM approach." The basic frequency-modulating wave is set to be the zero-point reference. As can be seen in Figure. 3 (a)the peak value of the carrier signals swings from 0 to +4 and from -4 to 0. The carrier group has a hierarchy on both the top and bottom of the zero frames. Therefore, if the modulating signal is greater than the carrier signal, the initial triggering signal is immediately created by comparing a sinusoidal modulating signal with a triangular carrier signal employing a comparator circuitry. The suitable switching signal for switching equipment is subsequently produced using the proper logical circuits. In the suggested arrangement with nine levels, Figure. 3(b) depicts the switching pulses associated with each of the switches.

## 4. Findings of ASRNLI Configuration

In MATLAB/SIMULINK, [14]-[15] the ASRNLI arrangement is developed and simulated using the LS-PDPWM technique for performance verification. The resulting 9-level waveform can be represented by voltages of 0, ±100V, ±200V, ±300V, and ±400V.




(a)




(b)

Figure.3. LS-PDPWM (a) Carrier set up (b) switching pulses

During the simulation investigation, specific parameters were considered, including a 200-ohm R load, V1=100V, and V2=300V. The results, along with the corresponding harmonic bands at a modulation index (MI) of 1, are illustrated in Figs. 4 and 5. At the peak fundamental voltage of 400V, the voltage and current output waveforms exhibit a Total Harmonic Distortion (THD) of 13.50%. Furthermore, Figs. 6 and 7 present the wave patterns of the voltage and current, along with the harmonic spectrum response for MI 0.95, respectively

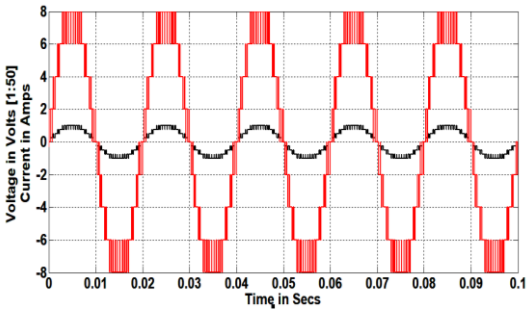



Figure. 4. PD Technique for R-load output voltage and current (modulation index 1)

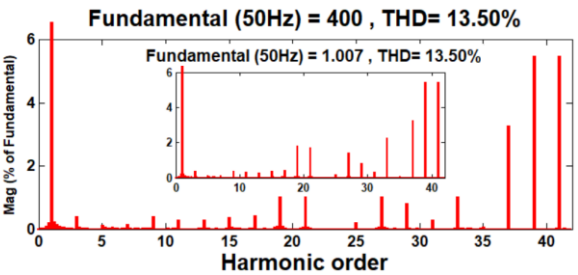



Figure.5.Voltage and Current THD for R load with modulation index 1

The ASRNLI system achieves a peak voltage of 359.9V, accompanied by a Total Harmonic Distortion (THD) of 16.68%. Figs. 8 and 9 showcase the waveform and harmonic voltage spectrum response for an MI of 0.9, respectively. The resulting waveform exhibits a total harmonic content of 16.99% and a peak fundamental voltage of 338.9V. Table II provides the performance factors associated with experimental results for modulation index (ma) values ranging from 0.9 to 1.

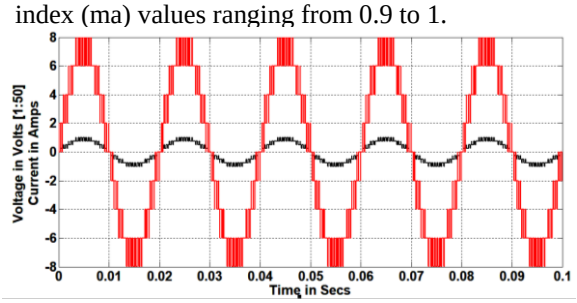



Figure.6.PD Technique for R-load output voltage and current (modulation index 0.95)

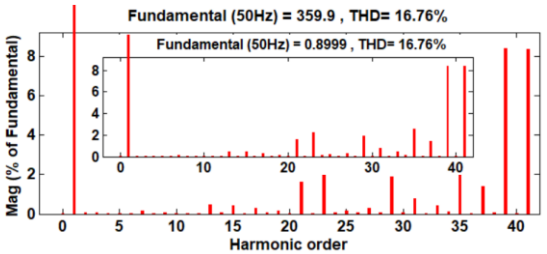



Figure.7.Voltage and Current THD for R load with modulation index 0.95

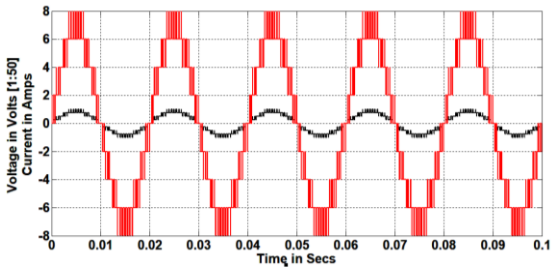



Figure.8.PD Technique for R-load output voltage and current (modulation index 0.9)

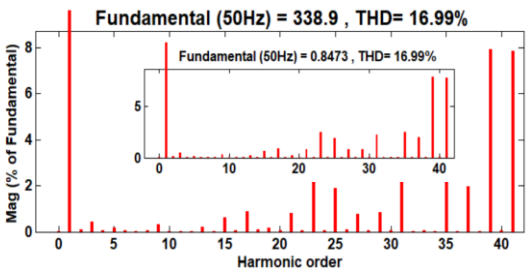



Figure.7.Voltage and Current THD for R load with modulation index 0.9

Table.2. Simulation results for R-load

| Ma | THD (V) | THD (I) | $V_{RMS}$ | $I_{RMS}$ |
|---|---|---|---|---|
| 1 | 13.50% | 13.50% | 283.6 | 0.709 |
| 0.95 | 16.99% | 16.99% | 269.1 | 0.6729 |
| 0.9 | 16.76% | 16.76% | 254.5 | 0.6364 |

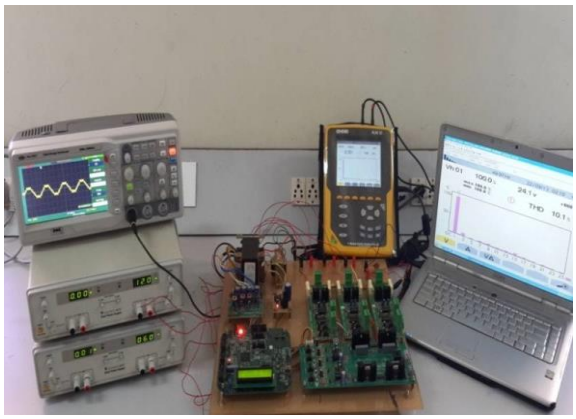


Figure.8. Prototype of ASRNLI

The results of the single phase nine level inverter experimental investigation with the SPARTAN-3 FPGA system are presented here. Since PWM controllers are commonly integrated into FPGAs, applicability is easy. Therefore, an FPGA is used to implement the ASRNLI in real time in this study. Multicarrier PWM control schemes for the selected inverter are generated with the help of Xilinix's system generator software. Hardware implementation involves compiling, bit-mapping, and downloading the gate signal generator model created by the system generator into a field-programmable gate array (FPGA). Through the input/output lines of the FPGA, the acquired pulses are sent to pulse amplifiers before being sent to the gates of IGBTs in the recommended inverter form. Figure. 8 depicts the hardware configuration. For experimentation, the following values are used: V1 = 100V, V2 = 300 V, R = 200 ohm. Table 3 displays the performance factors associated experimental results for ma values between 0.9 and 1.

Figs. 9 and 10 display the results form and the associated harmonic bands with a modulation index (MI) of 1. At a highest fundamental voltage of 399.8V, the voltage and current output waveform have a THD of 15%. Figures. 11 and 12 depict the wave patterns of the voltage and current in addition to the harmonic spectrum response for MI 0.95, accordingly. The peak voltage of the ASRNLI system is 349.9V, with an 18.9 % THD. The waveform produced and spectrum response of the harmonic voltage for MI of 0.9 have been portrayed in Figs. 13 and 14, correspondingly. The resultant waveform exhibits a total harmonic content of 19.5 % and a highest fundamental voltage of 331.9V.

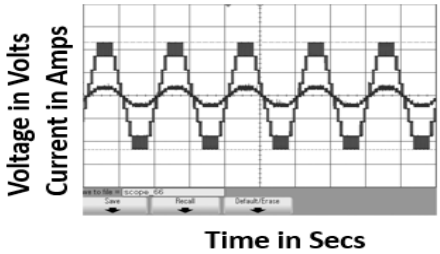



Figure. 9. PD Technique for R-load output voltage and current (Experiment - modulation index 1)

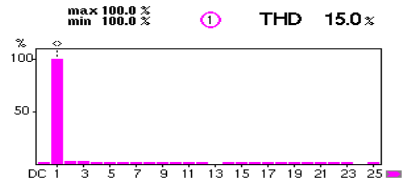



Figure. 10. THD for R load with modulation index 1

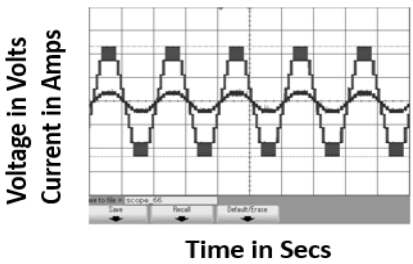



Figure. 11. PD Technique for R-load output voltage and current (Experiment - modulation index 0.95)

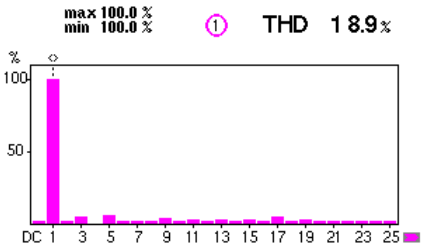



Figure. 12. THD for R load with modulation index 0.95

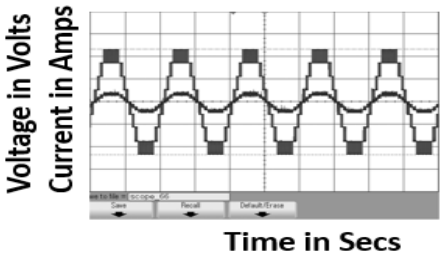


Figure. 13. PD Technique for R-load output voltage and current (Experiment - modulation index 0.9)

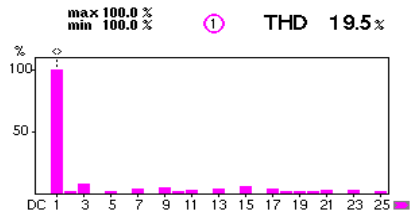



Figure. 14. THD for R load with modulation index 0.9

Table.3.Experimental Results for R-load

| Ma | THD(V) | THD(I) | VRMS | IRMS |
|---|---|---|---|---|
| 1 | 15% | 15% | 280.6 | 0.6909 |
| 0.95 | 19.5% | 19.5% | 260.1 | 0.6129 |
| 0.9 | 18.9% | 18.9% | 251.5 | 0.5964 |

## 5. Conclusions

This article presents a novel MLI design aimed at achieving the highest-level count while minimizing the number of switching power components and DC power supplies. Additionally, to enhance the output voltage's quality, a carrier pulse width modulation method has been applied. The recommended inverter utilizes the PD level-shifted PWM method, which has proven successful in generating a 9-level voltage output pattern using only 9 switches and 2 DC supplies. The DC source strengths follow a ternary series of increasing magnitude. Simulation testing and laboratory-based experiments with an R load were conducted to verify the effectiveness of the suggested ASRNLI architecture. The results and discussions indicate a significant impact on both the inverter's and the output voltage's harmonic spectra. Moreover, the proposed design is well-suited for both medium-power and low-power applications. Furthermore, the configuration exhibits scalability by easily cascading additional units, enabling it to expand into a modular n-level structure, thus offering potential enhancements for future implementations.

## Nomenclature

| | |
|---|---|
| *ASRNI* | asymmetrical single-phase nine level inverter |
| *CHB* | Cascaded H-Bridge inverter |
| *DC* | Direct Current |
| *FPGA* | Field programmable gate array |
| *PWM* | Pulse width modulation |
| *THD* | Total harmonic distortion |
| *LS-PD* | Level shift phase disposition |
| *Vrms* | Root mean square voltage |
| *Irms* | Root mean square current |

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