Journal of Solar Energy Research (JSER)

Journal homepage: jser.ut.ac.ir

A New L-C-D Cell Based Non-Isolated Single Switch High Step-Up DC-DC Converter for Photovoltaic Applications

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Received: 2021-10-25
Accepted: 2022-06-25

Abstract

This paper proposes a new non-isolated single switch boost DC-DC converter for high voltage applications. The proposed converter combines the conventional boost converter with two inductor-capacitor-diode (L-C-D) cells and achieves non-inverting high voltage gain without using a high duty cycle. Additionally, the proposed topology presents a continuous input current that makes it suitable for renewable energy applications, such as photovoltaic systems. The absence of a transformer, using devices with low voltage rating, low voltage stress across the semiconductors, no voltage spike on the switches, and common ground between source and load terminals are advantages of the proposed converter. The principles of the operation in three different modes are analyzed. In addition, the design considerations for the proposed converter are discussed. The main parameters of the converter like the voltage gain and the voltage stress on the diodes and switches are calculated and then compared with other solutions introduced in previous works. Finally, a 400W/200V experimental prototype is designed and experimentally tested. The experimental results demonstrate the effectiveness of the proposed converter.

Keywords Boost dc-dc converter, High voltage gain, Low voltage stress, photovoltaic

1 Introduction

Recently, many researchers present different non-isolated DC-DC converters with simple and robust topologies to provide high voltage gain for various applications such as photovoltaic (PV) systems, energy storage systems, wind turbines (WT), fuel cells (FC), hybrid electric vehicles, DC distribution systems, and uninterruptable power supplies (UPS) [1]. Renewable energy sources have some limitations such as Low output voltage. Theoretically, a conventional boost DC–DC converter can provide high voltage gain at high duty cycles. But, in practice, the losses of the equivalent series resistances (ESR) of passive components and parasitic elements of semiconductors, reduce the voltage gain [2]. However, the main issue relevant to DC-DC converters with high voltage gain is the quality of the input current waveform and lower manufacturing and operational costs. Recently, in high step-up DC-DC converter applications, the high voltage gain, high efficiency, and reduced voltage stress on devices are the main objectives which have been discussed in literature. These converters can be generally categorized into with and without coupled inductor. The major drawbacks of the topologies with coupled inductor are leakage inductance, large voltage spikes across the switches, noticeable EMI, and low efficiency of the converter [3].

In [4] and [5] high voltage gain DC-DC converters with coupled inductor are proposed. The leakage inductance is the main disadvantage of these structures, which causes the voltage stress and high voltage spikes on semiconductors. In order to solve this problem, the stored energy in the leakage inductance must be dissipated using additional snubber circuits. Large number of devices in a converter circuit, increases the complexity, size and cost of the converter [6].

The non-coupled inductor DC-DC converters are upgraded using conventional boost converter together with an extra method associated. The most practical techniques used include voltage multiplier cells [3,7], switched-capacitor and switched-inductor cells [8,9], cascaded boost converters [10], and combinations of above methods [11]. The aforementioned converters are capable to improve the conversion efficiency and provide high step-up voltage gain without using isolated transformer and coupled inductor techniques. However, high number of components in a converter increases the cost and complexity and reduces the efficiency.

A hybrid switched-inductor boost converter is investigated in [12]. This converter can achieve a large conversion ratio with a network of active and passive switched inductors. The disadvantages of this converter are; PWM voltage difference at high frequency between the input voltage source and load side and utilization of two power switches. Another technique for improving high-voltage conversion ratio in DC-DC converters is voltage-lift (VL) technique [13]. This converter has a low voltage stress on the power switch and common ground between source and load terminals. Disadvantages of this converter are using an additional input filter, high input current ripple, and increasing weight and size of the converter. Cascading of the boost converter with several voltage multiplier cells is another technique for increasing the voltage gain. However, as the number of multiplier cells increases, the complexity of the control system, the conduction loss, and the system size are increased [3,14].

DC-DC boost converter based on the diode-capacitor multiplier cell can achieve large voltage gain, low input current ripple, and low voltage stress across the switch [15]. Major disadvantages of this converter is that the voltage gain and efficiency decrease and the conduction losses of the diodes increase because of increasing number of multiplier cells. Different impedance networks like quasi-Z-source [16] and the switched-inductor Z-source [17] have been constructed and applied to boost converters to improve the voltage gain. Although, the aforementioned Z-source-based converters suffer from the large number of additional electronic components. In the switched capacitor (SC) based converters [18], the voltage gain is increased by combining a number of switches and capacitors with minimum inductors. In recent years, switched capacitor (SC) technique has been developed to achieve high efficiency and high voltage gain [19]. However, in this converter the number of capacitors and switches are increased, and consequently the losses and switching current ripple are increased. In [20], a SC converter has been introduced which reduces the switching control complexity and current ripple by combining a number of capacitors and diodes. In [21], by using a coupled inductor in the SC cell, the conduction losses on the power switches and elements have been decreased. In [22], a non-isolated high step-up DC-DC converter with switching capacitors has been proposed which charges n capacitors up to input voltage and connect them in series to boost the voltage. However, the high switching losses on the last switch and need to several switches are the main disadvantages. Combination of the conventional boost converter with switching capacitors has been investigated in [23]. Another solution to achieve high voltage gain is the quadratic boost converter [24], but filter capacitors and additional inductors must be used and the voltage of the switch is high. Different boosting techniques for achieving high step-up voltage gain in DC-DC converters have been reviewed in [25].

In this paper, a single-switch non-isolated high-voltage gain DC-DC converter is proposed. The suggested converter uses inductor-capacitor-diode (L-C-D) circuit to provide larger voltage gain. The configuration and operational modes of the proposed converter illustrate in section 2. Section 3 explains the analysis and design considerations for the converter. A comparative study between seven high voltage gain DC-DC boost converters without magnetic coupling components is performed in section 4. The experimental results for a 400W prototype of the proposed converter are given and analyzed in section 5. Finally, section 6 concludes the paper.

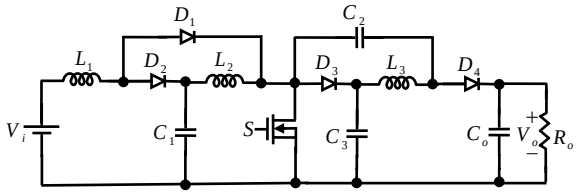


Fig. 1 Proposed DC-DC converter

2. CIRCUIT CONFIGURATION AND OPERATIONAL MODE ANALYSIS

2.1 Circuit Configuration

In order to enhance the voltage-gain of a step-up DC-DC converter and to reduce the voltage stress across its power semiconductors, a conventional boost DC-DC converter is combined with two $L-C-D^2$ and $L-C^2-D$ networks. Fig. 1 shows the circuit configuration of the proposed converter. It consists of one switch (S), four diodes (D_1 – D_4), three inductors (L_1 – L_3), four capacitors (C_1 – C_4) and the resistive load (R_o). The conventional boost converter consists of (L_1 , S , D_4 , and C_o), and two $L-C-D^2$ and $L-C^2-D$ networks are formed by (L_2 , L_3 , C_1 , C_2 , C_3 , D_1 , D_2 , and D_3). To simplify the circuit analysis, the following assumptions are considered; 1) The converter components are ideal; 2) The switching frequency is constant; 3) The capacitors are large enough so that their voltages can be assumed constant in each switching cycle.

2.2 Operational Modes of the Proposed Converter

The operation of the proposed converter is investigated in three different modes: continuous conduction mode (CCM), discontinuous conduction mode (DCM), and boundary conduction mode (BCM).

2.2.1 CCM Operation

In this mode, the operating of the converter in a switching period of T_S can be divided into two time intrevals. In the first time interval, the switch S is in on state ($S=1$) and in the second time interval, the switch S is in off state ($S=0$). Operating principles and analysis of the converter during these two time intervals are explained as follows:

i) Mode I [$0 \le t < DT_S$]

In this time interval, as shown in fig. 2(a), switch S and diode D_1 are in on state, while diodes D_2 , D_3 and D_4 are in off state. The source energy is transferred to the inductor L_1. The capacitors C_1 and C_3 transfer the energy to the inductors L_2 and L_3, respectively and the capacitor

C_2 is charged. In this mode, the following equations achieves:

$$-v_{C1}+v_{L2}-v_{C2}-v_{L3}+v_{C3}=0 \quad (1)$$

$$v_{L1}=V_i \quad (2)$$

$$v_{L2}=v_{C1} \quad (3)$$

$$-v_{C2}-v_{L3}+v_{C3}=0 \quad (4)$$

ii) Mode II [$DT_S \le t < T_S$]

The equivalent circuit of the proposed converter in second time interval is illustrated in Fig. 2(b), where switch S and diode D_1 are in off state and diodes D_2 , D_3 and D_4 are in on state. The current of inductors L_1 , L_2 and L_3 are linearly decreased. In addition, the capacitors C_1 and C_3 are charged and the capacitor C_2 is discharged and provides its energy into inductor L_3 . Thus, the related equations can be written as follows:

$$V_i = v_{L1}+v_{C1} \quad (5)$$

$$v_{L3}=-v_{C2} \quad (6)$$

$$-v_{C1}+v_{L2}+v_{C3}=0 \quad (7)$$

$$-v_{C3}+v_{L3}+V_o=0 \quad (8)$$

In the continuous current mode, considering the voltage balancing role, the average voltage of the inductors L_1 , L_2 and L_3 are zero in each switching period. Thus, using equations (1)-(8), the following equations are obtained:

$$\frac{1}{T_S}\left(\int_0^{DT_S} V_i dt+\int_{DT_S}^{T_S}(V_i-v_{C1})dt\right)=0 \quad (9)$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} v_{C1} dt+\int_{DT_S}^{T_S}(v_{C1}-v_{C3})dt\right)=0 \quad (10)$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} (v_{C3}-v_{C2})dt+\int_{DT_S}^{T_S}(-V_o+v_{C3})dt\right)=0 \quad (11)$$

By solving (9)-(11), we have:

$$v_{C1}=(1-D)v_{C3}=\frac{V_i}{(1-D)} \quad (12)$$

$$v_{C2}=v_{C3}-v_{C1}=Dv_{C3}=\frac{DV_i}{(1-D)^2} \quad (13)$$

$$v_{C3}=\frac{V_i}{(1-D)^2} \quad (14)$$

Using equations (12)-(14), the voltage-gain (M_{CCM}) can be written as (15).

$$M_{CCM}=\frac{V_o}{V_i}=\frac{1+D}{(1-D)^2} \quad (15)$$

If the power circuit contains lossless elements, then the average input current can be calculated according to (16).

$$I_i=\frac{1+D}{(1-D)^2}I_o \quad (16)$$

In mode I, the capacitor C_o is discharged by turning on the switch and in mode II, it is charged by turning off the switch.

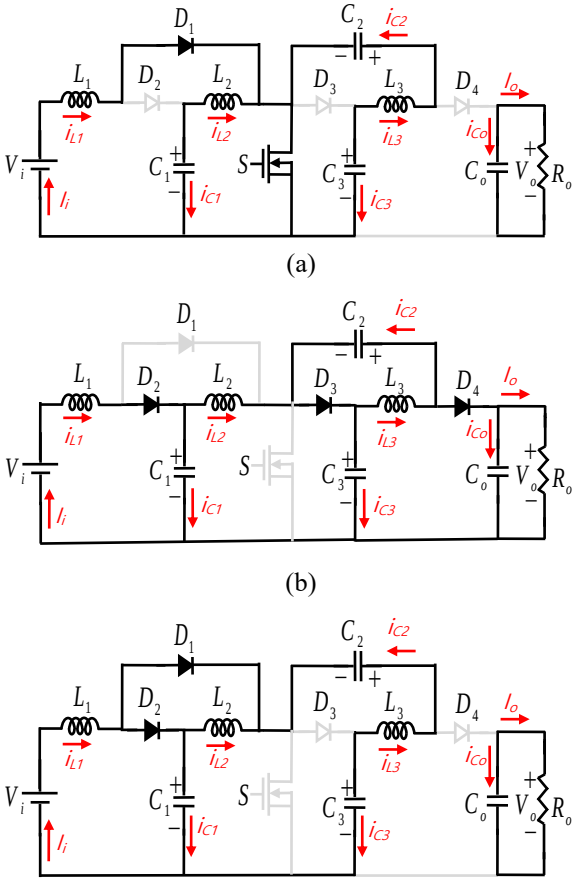


Fig. 2 Equivalent circuit models of the proposed converter. **(a)** mode I, **(b)** mode II, **(c)** mode III for DCM operation.

Therefore:

$$Q_{C_o^-}=I_o DT_S \quad (17)$$

$$Q_{C_o^+}=I_{C_o-off}(1-D)T_S \quad (18)$$

In a switching cycle, $Q_{C_o^+}=Q_{C_o^-}$. So, we have:

$$I_{C_o-off}=\frac{D}{1-D}I_o \quad (19)$$

It is clear that during switching-off, $i_{D4}=i_{Co}+I_o$, therefore

$$I_{D_4-off}=I_{D_3-off}=I_{C_o-off}+I_o=\frac{1}{1-D}I_o \quad (20)$$

2.2.2 DCM Operation

In DCM mode, the diode D_4 is reversely biased and current i_{D4} reduces to zero during the switch-OFF period. Therefore, there are three different operational modes related to three time intervals. Mode 1 and mode 2 are similar to the first and second modes in CCM operation. In the third time interval (Fig. 2(c)), the power switch S and the diodes D_3 and D_4 are turned OFF and the voltage across the inductors L_2 and L_3 are approximately zero. The essential waveforms under DCM operation are shown in Fig. 3(b).

Using the charge balance principle for C_1, C_2, C_3 and C_o, the charging and discharging currents of the capacitors, are extracted as follows:

$$\left.\begin{aligned} &i_{C1-dis}\times DT = i_{C1-ch}(1-D)T \\ &i_{C2-ch}\times DT = i_{C2-dis}(1-D)T \\ &i_{C3-dis}\times DT = i_{C3-ch}(1-D)T \\ &i_{Co-dis}\times DT = i_{Co-ch}(1-D)T \end{aligned}\right\} \tag{21}$$

$$\left.\begin{aligned} &i_{C1-ch} = I_{L1}-I_{L2} = \frac{I_o(D^2+D)}{(1-D)^2} \\ &i_{C1-dis} = -I_{L2} = -\frac{(1+D)}{(1-D)}I_o \end{aligned}\right\} \tag{22}$$

$$\left.\begin{aligned} &i_{C2-ch} = I_{L3} = I_o \\ &i_{C2-dis} = I_{L3}-I_{L2}+i_{C3-ch} = \frac{-D}{(1-D)}I_o \end{aligned}\right\} \tag{23}$$

$$\left.\begin{aligned} &i_{C3-ch} = I_{L2}-I_{L3}+i_{C2-ch} = \frac{D}{(1-D)}I_o \\ &i_{C3-dis} = -I_{L3} = -I_o \end{aligned}\right\} \tag{24}$$

$$\left.\begin{aligned} &i_{Co-ch} = I_{L3}-i_{C2-dis}-I_o = -\frac{D}{(1-D)}I_o \\ &i_{Co-dis} = -I_o \end{aligned}\right\} \tag{25}$$

Δi_{L1}, Δi_{L2} and Δi_{L3} are the ripple currents of the inductors (L_1,) and can be calculated as follows: $L_{\backslash}$ and $L_{\backslash}$

$$\Delta i_{L1} = \frac{v_{L1}}{L_1}DT_S = \frac{DV_i}{(1-D)f_S\ L_1} \tag{26}$$

$$\Delta i_{L2} = \frac{v_{L2}}{L_2}DT_S = \frac{v_{C1}}{L_2}DT_S = \frac{DV_i}{(1-D)\,f_S\ L_2} \tag{27}$$

$$\Delta i_{L3} = \frac{v_{L3}}{L_3}DT_S = \frac{(v_{C3}-v_{C2})}{L_3}DT_S = \frac{DV_i}{(1-D)\,f_S\ L_3} \tag{28}$$

Using (27) and (28), the peak current of D_3 and D_4 can be obtained as (29).

$$i_{d3.\max} = i_{d4.\max} = \frac{\Delta i_{L2}+\Delta i_{L3}}{2} = \frac{DT_SV_i}{2(1-D)L_{eq}} \tag{29}$$

$$L_{eq} = \left[\frac{1}{L_2}+\frac{1}{L_3}\right]^{-1} \tag{30}$$

The average value of the diode current i_{D4} equals I_o, hence, it can be written as:

$$< i_{D4} >= \frac{1}{T}\left(\frac{\Delta T}{2}\frac{DV_i}{2(1-D)\,f_SL_{eq}}\right) = \frac{V_o}{R} \tag{31}$$

Hence, Δ can be extracted as in (32):

$$\Delta = \frac{4(1-D)\,f_SL_{eq}V_o}{DV_iR} = \frac{4(1-D)V_o}{DV_i}K \tag{32}$$

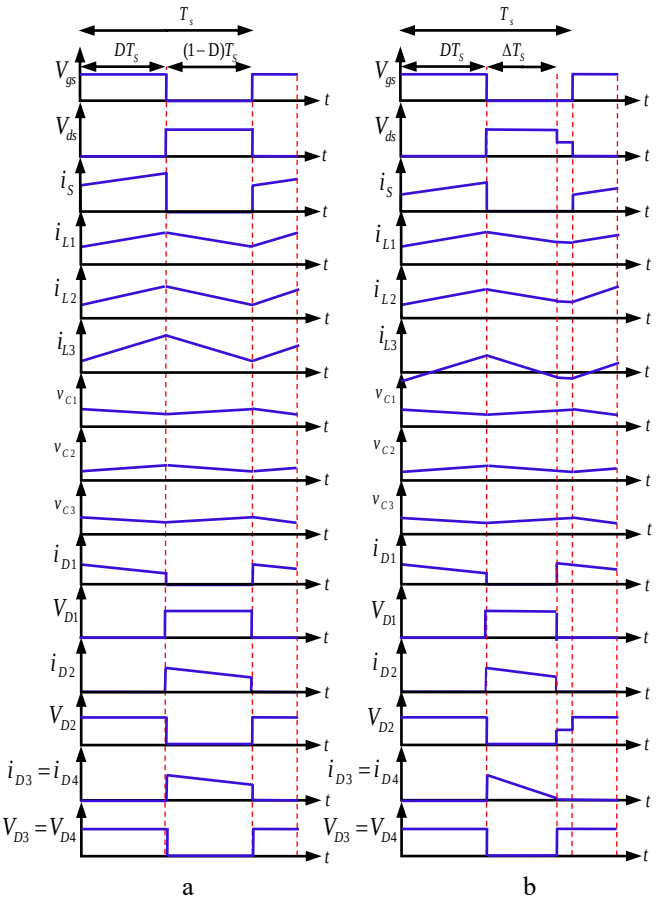


Fig. 3 Essential waveforms of the proposed converter **(a)** operation in CCM, **(b)** operation in DCM.

where the dimensionless parameter K is defined by (33).

$$K = \frac{f_SL_{eq}}{R} \tag{33}$$

According to flux balance, the average voltage of the inductors should be zero at the steady-state condition. Therefore, the following equations can be obtained:

$$\frac{1}{T_S}\left(\int_0^{DT_S} V_i dt + \int_{DT_S}^{(D+\Delta)T_S}(V_i - v_{C1})dt\right) + \int_{(D+\Delta)T_S}^{T_S}(V_i - v_{C1})\,dt = 0 \tag{34}$$

$$\frac{1}{T_S}\left(\int_0^{DT_S} v_{C1}dt + \int_{DT_S}^{(D+\Delta)T_S}(v_{C1}-v_{C3})dt\right) + \int_{(D+\Delta)T_S}^{T_S} 0\,dt = 0 \tag{35}$$

$$\frac{1}{T_S}\left(\int_0^{DT_S}(v_{C3}-v_{C2})dt + \int_{DT_S}^{(D+\Delta)T_S}(-V_o+v_{C3})dt\right) + \int_{(D+\Delta)T_S}^{T_S}(v_{C3}-v_{C2}-v_{C1})\,dt = 0 \tag{36}$$

Using (34), (35) and (36), the voltage of C_1, C_2 and C_3 can be calculated by (37), (38) and (39), respectively:

$$v_{C1} = \frac{V_i}{(1-D)} \tag{37}$$

$$v_{C2} = v_{C3} - v_{C1} = \frac{D}{\Delta} v_{C1} = \frac{D}{\Delta(1-\mathrm{D})} V_i \tag{38}$$

$$v_{C3} = \frac{(\Delta + D)}{\Delta} v_{C1} = \frac{(\Delta + D)}{\Delta(1-D)} V_i \tag{39}$$

Using (34)-(39), the voltage gain in DCM operation is obtained as follows:

$$M_{DCM} = \frac{V_o}{V_i} = \frac{2D + \Delta}{\Delta(1-D)} \tag{40}$$

Replacing (32) into (40), the voltage gain in DCM operation can be rewritten as:

$$M_{DCM} = \frac{V_o}{V_i} = \frac{1 + \sqrt{1 + \frac{2D^2}{K}}}{2(1-D)} \tag{41}$$

2.2.3 Boundary operation condition

The critical value of K ($K_{critical}$) versus D at the boundary conduction mode (BCM) has been illustrated in Fig. 4. During BCM operation, the voltage gains of the CCM and DCM operations are the same.
From (15) and (40), $K_{critical}$ can be derived as follows:

$$K_{critical} = \frac{D^2}{2(1+D)-1} \tag{42}$$

In Fig. 4, when $K < K_{critical}$ the converter works in DCM, otherwise it works in CCM.

3. DESIGN CONSIDERATIONS FOR THE COMPONENTS

In this section, the design considerations for the proposed converter in CCM operation are illustrated in detail and the results are validated using experimental results in section 5.

3.1 *Voltage Stress Across Switches and Diodes*

From Fig. 3, the voltage stress on the switch (V_{ds}) is given by (43).

$$V_{ds} = v_{C3} = \frac{V_i}{(1-D)^2} \tag{43}$$

From Fig. 2(a) and Fig. 2(b) and according to (37)-(39) the voltage stress on the diodes D_1 , D_2 , D_3 and D_4 are calculated as follows:

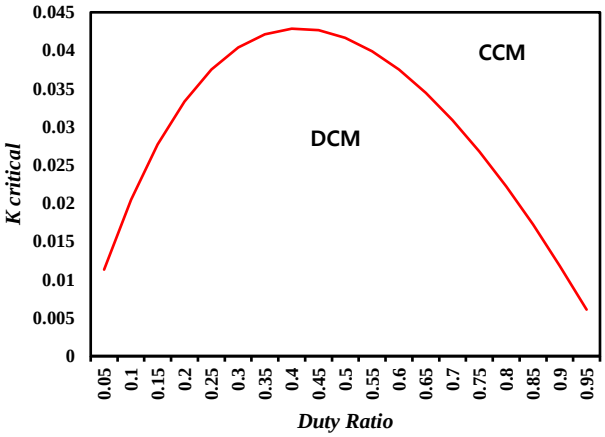


Fig. 4 Characteristic curve of the boundary conduction mode (BCM)

$$v_{D1} = \frac{D}{(1-D)^2} V_i \tag{44}$$

$$v_{D2} = \frac{V_i}{(1-D)} \tag{45}$$

$$v_{D3} = \frac{V_i}{(1-D)^2} \tag{46}$$

$$v_{D4} = V_o - \frac{DV_i}{(1-D)^2} \tag{47}$$

3.2 *Inductor Design*

The values of the inductances are depended on their voltage (V_L), duty cycle (D), switching frequency (f_S) and current ripple (Δi_L) [23]. In mode I, the voltage of the input inductance (L_1) is equal to V_i . Thus, the inductance value of L_1 is obtained as follows:

$$L_1 = \frac{DT_S V_i}{\Delta i_{L1}} \tag{48}$$

According to (3) and (12), the voltage of L_2 is equal to $V_i/(1-D)$ in mode I. Therefore, the inductance value of L_2 can be calculated using (49).

$$L_2 = \frac{DT_S V_i}{(1-D)\Delta i_{L2}} \tag{49}$$

Finally, according to (4), (13) and (14) the voltage of L_3 is also equal to $V_i/(1-D)$ in mode I. Therefore, the value of L_3 can be calculated as follows:

$$L_3 = \frac{DT_S V_i}{(1-D)\Delta i_{L3}} \tag{50}$$

3.3 *Capacitor Design*

The output capacitance value depends on four factors: the output power P_o , switching frequency f_S , output voltage ripple ΔV_C and output voltage V_o [26]. It can be expressed as:

$$C_o = \frac{DI_o}{\Delta V_{Co} f_S} \quad (51)$$

The voltages of capacitors $C_1 - C_3$ are calculated using (12)-(14). The peak-to-peak voltage ripples of the capacitors C_1, C_2 and C_3 (ΔV_{C1}, ΔV_{C2} and ΔV_{C3}) are known, thus the minimum values of capacitances can be expressed by (52)-(54):

$$C_1 = \frac{D(1-D^2)I_o}{(1-D)^2 \Delta V_{C1} f_S} \quad (52)$$

$$C_2 = \frac{DI_o}{\Delta V_{C2} f_S} \quad (53)$$

$$C_3 = \frac{DI_o}{\Delta V_{C3} f_S} \quad (54)$$

3.4 *Current Stress of the Components*

Assuming ideal components, the input and output powers of the converter are equal, i.e. $V_i \times I_i = V_o \times I_o$. I_{L1} is equal to the input current and I_{L3} is equal to the output current and substituting them into the expression (16), we have:

$$I_{L3} = I_o = \frac{V_o}{R} \quad (55)$$

$$I_{L1} = M_{CCM} I_{L3} = \frac{1-D^2}{(1-D)^3} \frac{V_o}{R} = \left(\frac{1-D^2}{(1-D)^3} \right)^2 \frac{V_i}{R} \quad (56)$$

Using equations (23)-(28) and Fig. 3, the current stress on the switch and diodes can be extracted as given by (57)-(61):

$$i_S = D(I_{L1} + I_{L2} + I_{L3}) = D(I_i + (1-D)I_i + I_o) \quad (57)$$

$$i_{D1} = DI_{L1} = DI_i = \frac{D(1-D^2)}{(1-D)^3} I_o \quad (58)$$

$$i_{D2} = (1-D)I_{L1} = DI_i = \frac{(1-D^2)}{(1-D)^2} I_o \quad (59)$$

$$i_{D3} = I_{L2} - i_{C2-dis} = \frac{1}{1-D} I_o \quad (60)$$

$$i_{D4} = I_{L3} + i_{C2-dis} = \frac{1}{1-D} I_o \quad (61)$$

3.5 *Efficiency Analysis*

The converter efficiency is considered as:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \quad (62)$$

The total power loss of the proposed converter is consist of the power losses of switch (P_{Loss}^S), diodes (P_{Loss}^D), capacitors (P_{Loss}^C), and inductors (P_{Loss}^L) and can be obtained as follows:

$$P_{Loss} = \sum (P_{Loss}^S + P_{Loss}^D + P_{Loss}^C + P_{Loss}^L) \quad (63)$$

The switching loss of the switch can be calculated using (64).

$$P_{Loss}^{S,switching} = \frac{1}{2} \Delta V_{DS} (I_{DS,on} t_r + I_{DS,off} t_{off}) f_S \quad (64)$$

The conduction loss of the switch can be calculated using (65).

$$P_{Loss}^{S,conduction} = R_{DS(on)} I_{DS,rms}^2 \quad (65)$$

In the above relationship, $R_{DS(on)}$ is ON-state resistance of the switch. Therefore, the total loss of the switch (P_{Loss}^S) contains the terms conduction and switching losses and can be expressed as follows:

$$P_{Loss}^S = P_{Loss}^{S,conduction} + P_{Loss}^{S,switching} \quad (66)$$

The conduction loss of each diode is as follows:

$$P_{Loss}^D = R_D I_{D,rms}^2 + V_f I_{D,avg} \quad (67)$$

Which V_f is the forward bias voltage and R_D is forward resistance of the diode. The power loss of each capacitor can be obtained by:

$$P_{Loss}^C = r_C I_{C,rms}^2 \quad (68)$$

Which r_C is the equivalent series resistance of the capacitor. The power loss of each inductor contains magnetic loss and conduction loss ($P_{Loss}^{L,conduction}$). The magnetic loss depends on the type of nucleus and the flux density ripple, which using datasheet provides necessary data. The conduction loss of the inductor can be calculated as follows:

$$P_{Loss}^{L,conduction} = r_L I_{L,rms}^2 \quad (69)$$

Where r_L is the equivalent series resistance of the inductors. When the output power of the converter is equal to 400 W, the efficiency is around 90.5% with total power loss being 40.6 W. Fig. 5 shows the efficiency of the converter at different load levels. Maximum efficiency of 94.1% is achieved at the output power level of 50 W.

4 COMPARATIVE STUDY

In Table 1. a comparative study between features of the proposed converter with other high voltage gain converters in [26]-[32] in terms of voltage gain, voltage stresses on the power switches and diodes, components count, and continuity of the input current is presented. The proposed converter has much higher voltage gain in comparison with other step-up converters. Fig. 6(b) shows the variation of the normalized voltage stress on the power switch in the proposed converter and other converters. As shown in Table 1, for lower number of elements compared to [28] and [30], the provided voltage gain of the proposed converter is higher. Other advantage of the proposed converter is continuous input current. Thus, it is suitable for renewable energy systems such as photovoltaic. Positive output voltage and absence of magnetic coupling elements are other advantages of the proposed converter.

5 EXPERIMENTAL RESULTS

In this section, a 400W laboratory prototype of the proposed converter as shown in Fig. 7 is built and tested. The parameters of the prototype converter and its specifications are listed in Table 2 and the experimental results are shown in Figs. 8–11. The converter switching is controlled with the microcontroller ATmega32 AVR. The proposed converter is operated in CCM operation mode. The experimental results are obtained in case of switching frequency is equal to 40kHz, the input voltage (V_i) is equal to 24V and the output voltage (V_o) is equal to 200V with a 56.94% duty cycle. According to (15), the voltage gain is approximately 8.46. Fig. 8(a) shows that the voltage gain

obtained in the experimental test, is near to the theoretically obtained voltage gain. According to (51), the converter operates in the least output voltage ripple condition (less than 1 V), thus the result is acceptable.

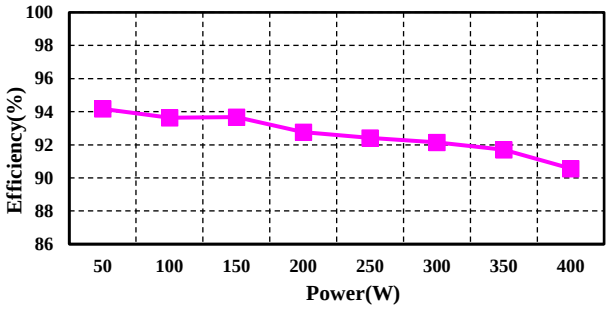
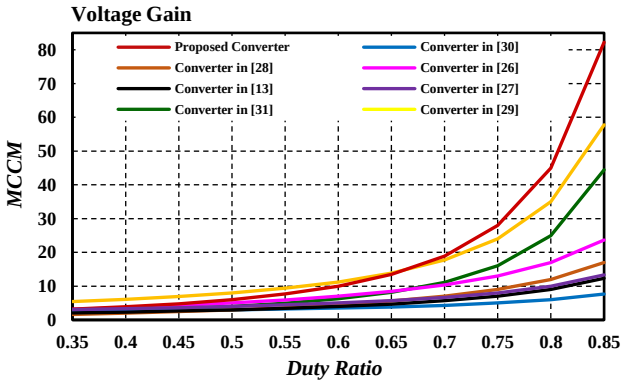
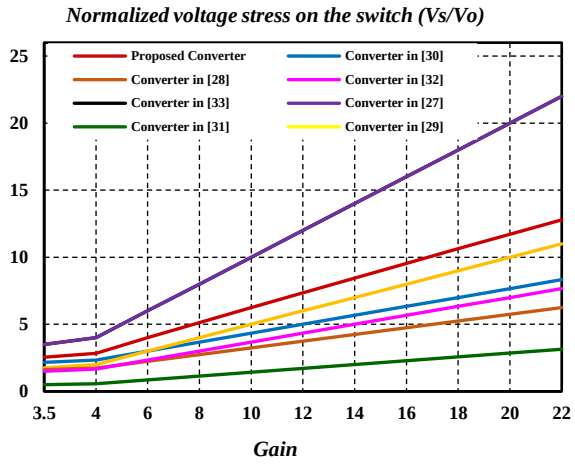


Fig. 5 Measured efficiency of the proposed converter



(a)



(b)

Fig. 6 Comparison among the proposed converter and some other structures (a) Voltage gain, (b) Normalized voltage stress on the switch.

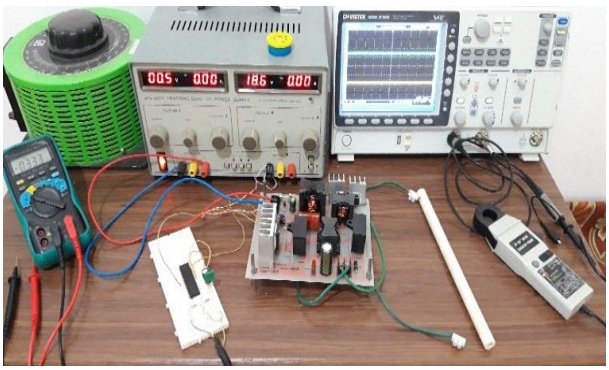


Fig. 7 Experimental setup of the proposed converter

Table 1 Comparative study between features of the proposed converter with other high voltage gain converters

Converter	Proposed	[33]	[32]	[31]	[30]	[29]	[28]	[27]
Voltage gain	$\frac{1+D}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{2+D}{1-D}$	$\frac{3-2D}{(1-D)^2}$	$\frac{3D}{1-D}$	$\frac{2}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{1+D}{1-D}$
Voltage stress on the switches	$\frac{V_o}{(1+D)}$	V_o	$\frac{V_o}{2+D}$	$\frac{V_o}{7}$	$\frac{V_o}{3D}$	$\frac{V_o}{2}$	$\frac{V_o}{(1+3D)}$	V_o
Maximum voltage stress on the diodes	$V_o - \frac{DV_i}{(1-D)^2}$	V_o	$\frac{V_o}{2+D}$	$\frac{V_o}{7}$	$\frac{V_o}{3D}$	$\frac{V_o}{2}$	$\frac{2V_o}{(1+3D)}$	V_o
Number of switches	1	1	1	1	1	1	2	1
Number of diodes	4	3	4	4	3	3	2	4
Number of inductors	3	2	2	1	4	2	3	2
Number of capacitors	3	2	5	4	6	4	3	3
Total device count	11	8	12	10	14	10	10	8
Continuous input current	Yes	Yes	Yes	No	Yes	Yes	No	Yes

Table 2 Specifications and parameters of the prototype converter

Symbol	Quantity	Value
P_o	Output power	400 W
V_i	Nominal input voltage	24 V
V_o	Output voltage	200 V
f_s	Switching frequency	40 kHz
L_1	Inductors	123 µH
L_2		80 µH
L_3		246 µH
C_1	Main capacitors	40 µF
C_2, C_3		10 µF
C_o	Output capacitor	150 µF
D_1, D_2	Diodes	U1560
D_3, D_4		MUR460
S	Switch	2SK3131

The output current is 2 A. Thus, the output power is about 400 W. Also, the average deviation between the theoretically and experimentally obtained voltage gains is about 2%.

The calculated voltage gain is different from the measured voltage gain because there are different power losses in the converter circuit such as diodes losses, MOSFET conduction loss and power losses due to the equivalent series resistance

of the inductors and capacitors. The output voltage V_o is presented in Fig. 8(a). According to Fig. 8(b), the input voltage V_i is 24 V. As shown in Fig. 9(a), the input current (I_i) which is equal to inductor (L_1) current, is continuous and is approximately 16.5 A with small ripples. Therefore, the proposed converter is convenient for use in renewable energy systems such as photovoltaic applications. The current and voltage stress of the switch S, achieved using (43) and (57). The voltage and current stress across the switch is respectively 128.1 V and 17.9 A. Thus, experimental results are close to the theoretical values, as shown in Fig. 8(c). Fig. 9(a) shows the voltage and current of the input inductor (L_1). Also, the current and voltage of the two inductors L_2 and L_3 are shown in Figs. 9(b)–(c), respectively. According to the converter parameters in Table 2 and equations (48), (49), (50), (55) and (56), the average currents of the inductors L_1, L_2, and L_3 are calculated as 16.2, 7.2, and 1.96 A, respectively. The current ripples of the inductors are approximately 2 A, which is small, as shown in Fig. 9. The equations (44)-(47) can be used to calculate the current and voltage stress of the diodes D_1, D_2, D_3, and D_4, which the results are experimentally verified as shown in Fig. 10.

As shown in Figs. 11(a)–(c), the voltage of capacitors C_1, C_2 and C_3 are equal to 54 V, 72 V and 127 V, respectively, which are agree with the results obtained by equations (12)-(14).

According to the above discussion, the experimental results for a 400W prototype validate the theoretical analysis. Therefore, the advantages such as high voltage gain and the reduced voltage stress on the switches are achieved in the proposed converter.

6. CONCLUSION

A new single switch non-isolated, high step-up DC-DC converter has been presented. A high voltage gain with a small duty cycle was achieved using two inductor-capacitor-diode (L-C-D) cells. Suggested converter has advantages such as simple control system, non-inverting output voltage, very high voltage gain without using any coupled inductors and transformers, and continuous input current. The design methodology and steady-state analysis of the proposed converter under CCM, DCM and BCM operation have been presented. The voltage gain, the voltage stress on the switches and diodes, the number of components and the input current continuity have been compared between the proposed converter and some other recent non-isolated high step-up converters. Also, the variation of the potential difference between the input and the output terminals is constant, thus it is best suited for renewable energy applications. Finally, the experimental results on a 400W laboratory prototype were presented to validate the advantages of the proposed converter.

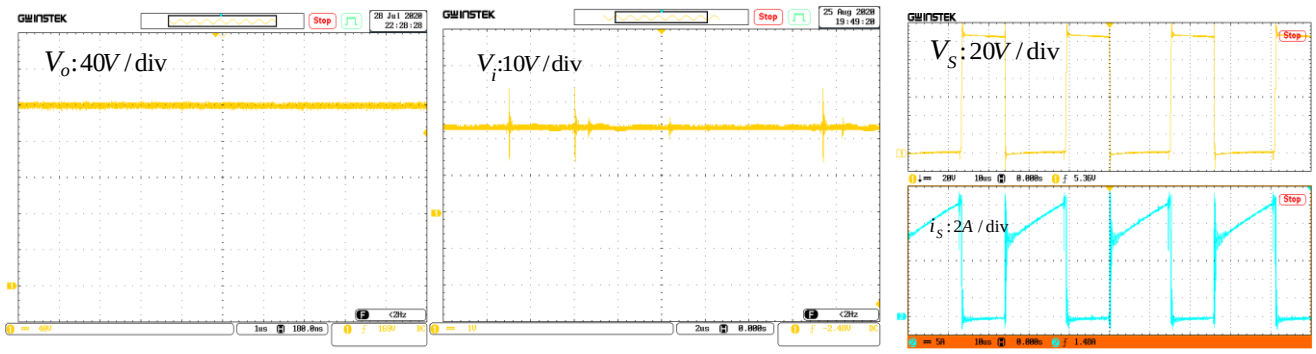


Fig. 8 Experimental results of the proposed converter **(a)** Output voltage, **(b)** Input voltage, **(c)** Voltage and current of the switch S

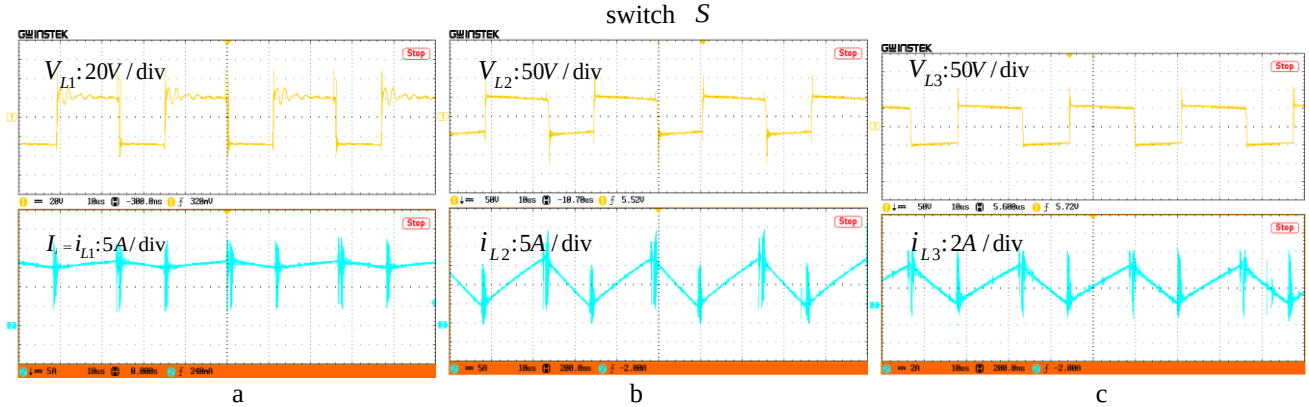
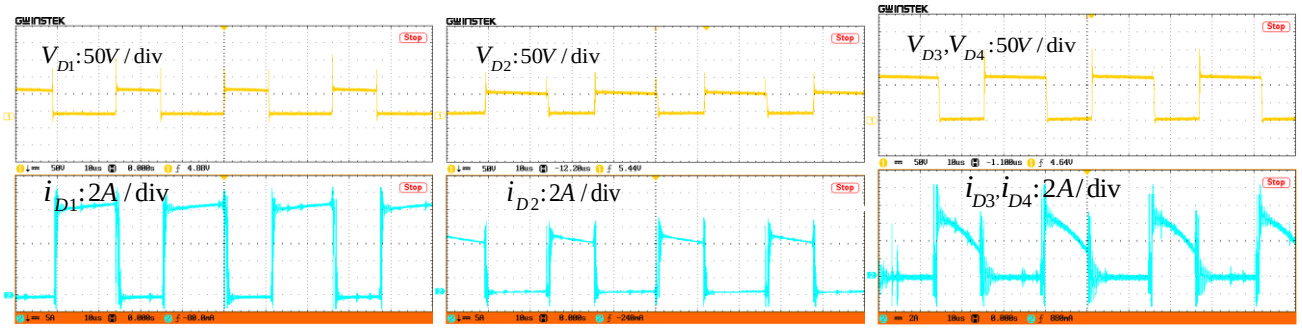
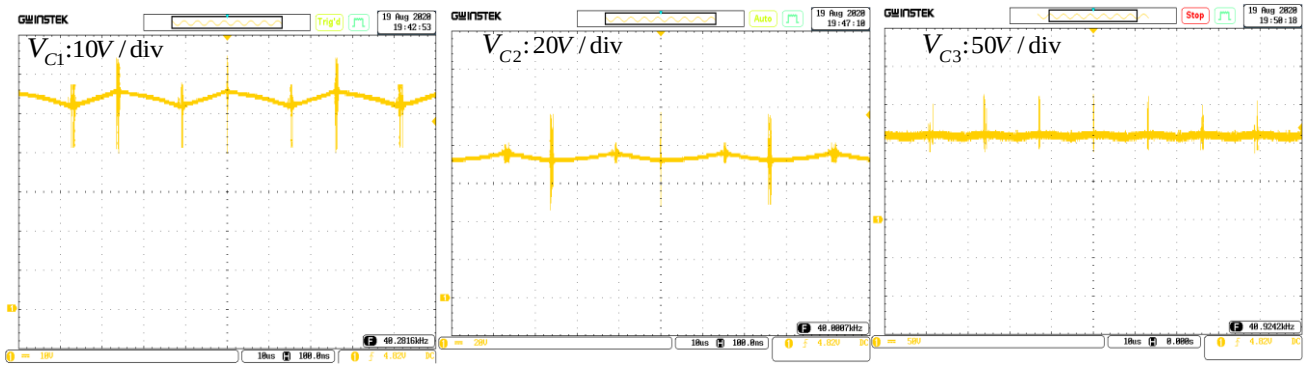


Fig. 9 Voltages and currents of the inductors **(a)** L_1, **(b)** L_2, **(c)** L_3.



a b c

Fig. 10 Experimental results for **(a)** voltage and current of diode D_1, **(b)** voltage and current of diode D_2, and **(c)** voltage and current of diode D_3.



a b c

Fig. 11 Experimental results for **(a)** voltage of capacitor C_1, **(b)** voltage of capacitor C_2, and **(c)** voltage of capacitor C_3

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