JSER

Journal of Solar Energy Research (JSER)

Journal homepage: www.jser.ut.ac.ir

A High-Gain Step up Converter for Solar Applications Based on PSOL Topology

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ARTICLE INFO

Received: 12 Jun 2019
Received in revised form:
24 Sep 2019
Accepted: 28 Oct 2019
Available online:
30 Oct 2019

Keywords:
Continuous Current Mode (CCM);
DC-DC Converter,
High Output Gain;
Luo Converter;
PSOL Converter

A B S T R A C T

DC-DC converters have found wide application in daily life due to considerable industrial requirements. However, high output gain in these converters is not achieved due to parasitic elements and other circuit restrictions. This shortcoming is very important for certain applications such as solar systems that need to boost considerably the low voltage output of PV panels. This paper proposes a new topology based on the PSOL converter that can increase output gain beyond a conventional PSOL converter. This topology benefits from clamp circuits and voltage multipliers that are efficiently added to a Luo converter to increase its output voltage gain. Circuit analysis both in continuous and discontinuous conduction mode is performed together with operational waveforms obtained by the simulation to show the performance of the proposed circuit. In addition, the proposed converter is compared against some of the conventional converters to show the superiority of the converter over other ones. The results show that the proposed converter can achieve higher gains in comparison with other methods. Meanwhile, the proposed topology utilizes a single switch to increase the output voltage. Finally, simulation results for 1 kW load are included in the paper to show the performance of the converter.

1. Introduction

Nowadays, renewable energy is used widely all around the world due to energy shortages and environmental pollution concerns about fossil fuels [1, 2]. Due to the stable operation and high efficiency, renewable energy systems are widely accepted as a source of energy [3-5]. However, these systems usually have low output voltage such as fuel cells and photovoltaic systems and need DC-DC converters with high output gain. Conventionally boost converters are adopted to increase the output voltage to the required levels that are used by electric consumers [6]. A typical fuel cell power supply system, with a super-boost converter, is shown in Figure 1.

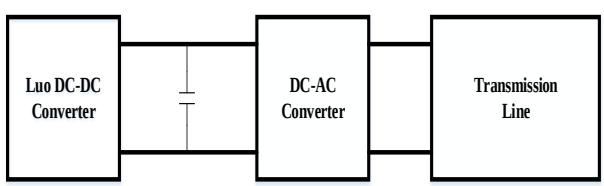

Figure 1. A conventional step up converter for renewable energy application

The fuel cells and solar cell voltage produced is relatively low [7-9]. Thus, for normal applications, a high output voltage is achieved by a high gain Luo converter that is connected to the Fuel cell. Finally, the output is

applied to an inverter to adapt it to the consumer voltage and frequency levels. Although a boost converter is deemed to have ideally infinite gain, some concerns reduce the practical gain according to the type of converters. Some of the affecting factors on the output gain are parasitic circuit resistances such as switch resistances, voltage transients in the circuit and switch voltage and current limits. Therefore, high output voltage gain is not easily possible with changing the duty cycle to its extreme limits [10]. Therefore, a gain of 10 times is typically high output gain among converters [11-12]. It is worth mentioning that this gain is achieved with only one switch in the circuit and therefore, in terms of the number of used switches it is superior to some of the topologies that use more than one switch [13].

In this paper, a converter named modified POSL is introduced that can develop output gain more than 12 times. This result is important since some previous work report a voltage boost of about 5 times for the PV applications that is much less than the proposed one [13]. The converter equations together with circuit waveforms that are found by simulation illustrate the performance of the converter. Some of the advantages of the converter are as follows:

- Voltage stress on the diodes and switch is much less than the output voltage
- Higher gain compared to conventional converters is achieved with a single switch

The proposed converter structure is presented in the next section and the various switching states it is analyzed. Then, the converter equations in continuous conduction mode (CCM) are discussed and finally, the simulation results are illustrated to show the performance of the converter.

2. POSL Converter Structure

Initial POSL converter structure [13] is shown in Figure 2. The converter is made of an inductor and two capacitors and two diodes and a single switch. According to the figure, when the switch S is on the diode D_1 conducts and diode D_2 is not conducting. The DC gain of the converter is equal to:

$$M(D)=\frac{V_o}{V_{in}}=\frac{2-D}{1-D} \qquad (1)$$

where D refers to the duty cycle.

In the above equation, D is the duty cycle of the power switch. This equation clearly shows that for large amounts of D converter operates like a classical boost converter. In this converter, when the switch is on, D_1 is conducting while D_2 is off and when the switch is off, D_2 is conducting while D_1 is off.

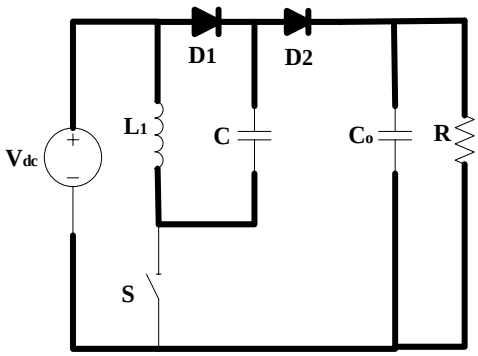

Figure 2. Structure POSL converter

3. Proposed Converter

The proposed converter structure is shown in Figure 3. This converter is actually developed by modifications in POSL to increase output voltage gain. In this structure, the combination of diodes and inductors (D_{34}, D_4, D_3, D_{12}, D_2, D_1, L_3,L_2,L_1) replace the inductor of the main PSOL circuit and the capacitors (C_2,C_1) are also utilized to clamp and boost output voltage. It is worth mentioning that the inductors (L_3, L_2, L_1) in the converter have magnetic coupling and L_1=L_2=L_3=L.

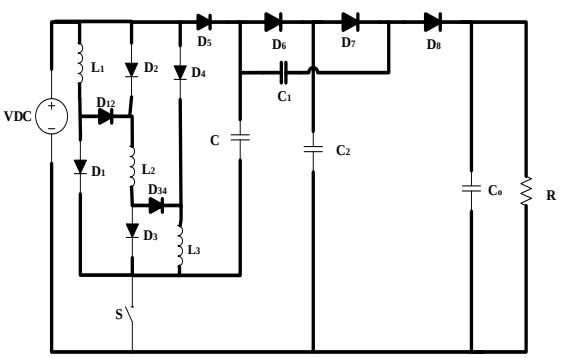

Figure 3. The structure of the proposed converter

The operation of the circuit is based on the status of the switch (S). the circuit starts as the switch (S) connects and makes the diodes (D_8,D_6,D_{34},D_{12}) to off state. In this case, the coupled inductors become in parallel and diodes (D_7,D_5,D_4,D_3,D_2,D_1) turn on. On the other hand, when the switch (S) disconnects, other diodes (D_8,D_6,D_{34},D_{12}) will

conduct and coupled inductors will become in series with the other elements of the circuit while previous diodes (D_7,D_5,D_4,D_3,D_2,D_1) will be off. The conduction path in these states is illustrated in Figure5.

4. Continuous Conduction Mode (CCM) Analysis of the Proposed Converter

In order to analyze the circuit operation in CCM, the converter current is assumed to be continuous and two intervals (switch on and off) are considered. According to Figure 4, In the first interval ($t_0 < t < t_1$) switch (S) is turned on (T_{On}) and in the second interval $t_1 < t < t_2$ and switch S is turned off (T_{Off}).

In the first interval [$t_0 < t < t_1$] diodes (D_7,D_5,D_4,D_3,D_2,D_1) are connected and inductors are connected in parallel with each other. Capacitors C and C_1 by diode D_7 and capacitors C_2 by the diode D_5 at the same time are charged. The equivalent circuit of the first interval is shown in Figure (5-a).

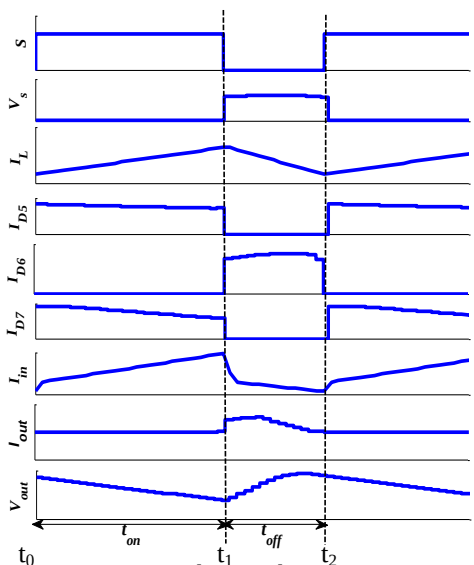

Figure 4. voltage and current Diagram

In the second interval ($t_1 < t < t_2$), Diodes (D_8,D_6,D_{34},D_{12}) are connected and the inductors are in series with each other while other diodes (D_5,D_4,D_3,D_2,D_1) are off. at the same time capacitor C_2 is charged by diode D_6 and output capacitor C_o is charged by the diode D_8 .the equivalent circuit of the first interval is shown in Figure (5-b).

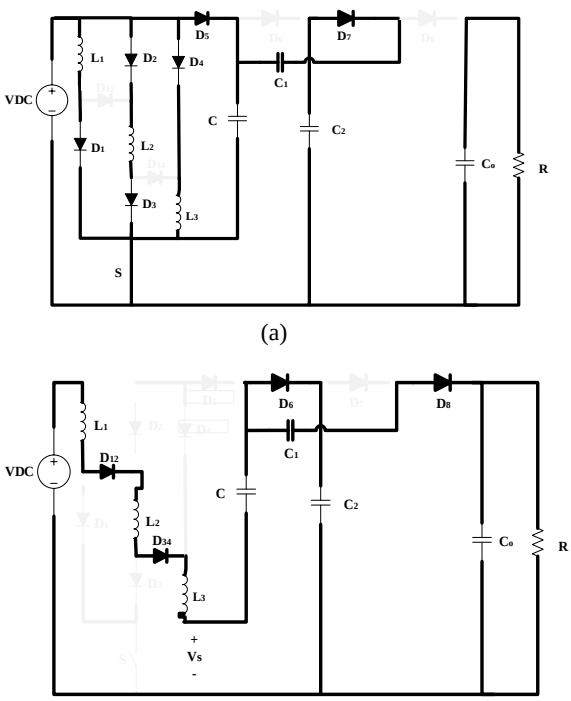

Figure 5. equivalent circuits of the proposed converter under CCM performance.

5. Discontinuous Conduction Mode (DCM) Analysis of the Proposed Converter

In this mode, circuit current (I_{min}) will reach zero. This means that inductor currents (L_3 ,L_2 , L_1) will be zero before switching period finishes at t_0. This phenomenon is depicted in Figure 6.

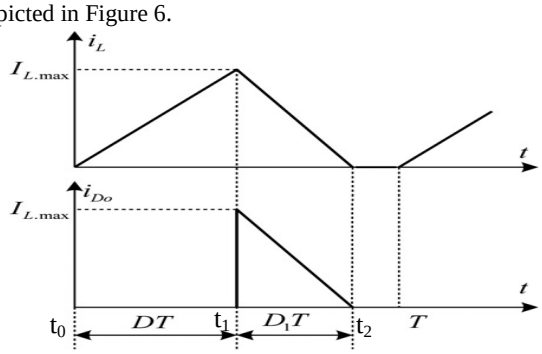

Figure 6. Chart of current in DCM

In this case $DT < t_2 < T$ and fill factor (m_L) is:

$$m_L = \frac{t_2 - DT}{(1-D)T} \quad (2)$$

Where $0<m_L<1$.

This means that the inductor current after the switch offwill go zero after m_L (1-D) T fill. In this case, Imin equal to zero and the average current I_L is equal to:

$$I_L = I_{\max}[D + D_1]/2 \quad and \quad \Delta i_L = I_{\max} \quad (3)$$

where Δi_L refers to maximum current fluctuations.

6. steady state analysis of the proposed converter

In this section, the analysis of the proposed converter is done in CCM. In addition, some basic assumptions are adopted as below:

- For simplicity voltage fluctuations are not considered.
- All of the components in the proposed converter are ideal.

6.1 Step-Up Gain

According to Figs. 5(a) and from the volt-sec balance of the inductors L_1 , L_2 , and L_3, the relation between the capacitor voltages in the first interval t_{on} = DT can be written as :

$$V_{L-on} = V_{in} = V_{L1} = V_{L2} = V_{L3} = V_c = (-V_{c1} + V_{c2}) \quad (4)$$

Where V_L refers to voltage across the inductor and V_c refers to voltage across the capacitor.

Also according to Figs. 5(a) and from the volt-sec balance of the inductors L_1 , L_2 , and L_3, the relationbetween the capacitor voltages the second interval t_{off} = (1-D)T:

$$-V_{in} + V_{L1} + V_{L2} + V_{L3} - V_c = 0 \quad (5)$$

the following equation is obtained:

$$V_{L-off} = -V_{in} + V_{L1} + V_{L2} + V_{L3} - V_c + (-V_{c1} + V_{out}) \quad (6)$$

Using the equations (4), (5) and (6) will result in:

$$V_{in} = (-V_{c1} + V_{c2}) \quad (7)$$

$$V_{c2} = (-V_{c1} + V_{out}) \quad (8)$$

$$V_{c1} = \frac{V_{out} - V_{in}}{2} \quad (9)$$

$$V_{L1} = V_{L2} = V_{L3} = \frac{2V_{in} - V_{out} + \frac{V_{out} - V_{in}}{2}}{3} \quad (10)$$

Where V_{in} and Vout refer to input and output voltage, respectively.

According to the volt-second balance law for inductors, there will be:

$$\frac{1}{T_s}\left(\int_0^{dT_s} V_{L\_on}\,dt + \int_{dT_s}^{T_s} V_{L\_off}\,dt\right) = 0 \quad (11)$$

$$V_{in}.DT = \left(\frac{2V_{in} - V_{out} + \frac{V_{out} - V_{in}}{2}}{3}\right)(1- \quad (12)$$

$$M(D) = \frac{V_o}{V_{in}} = \frac{3(D+1)}{1-D} \quad (13)$$

Generally, if n inductors are used, the following voltage gain is obtained:

$$M(D) = \frac{V_o}{V_{in}} = \frac{(2n-3)(D+1)}{1-D} \quad (14)$$

Voltage gain curve of the base converter and proposed converter versus the duty cycles of converters in CCM is shown in Figure 7. In this diagram, the proposed converter performance compared with the basic converter and converters proposed in reference [14] is much superior especially in high duty cycles.

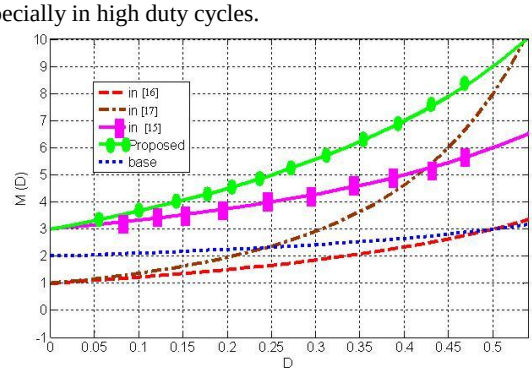

Figure 7. Gain voltage curve of the base converter and proposed converter relative to the duty cycle in CCM

One of the main points in the converter analysis is to find boundary conditions between CCM and DCM. The first step is to determine the input current. the inductor current is calculated as:

$$M(D) = \frac{I_{in\_ave}}{I_{o\_ave}} = \frac{3(D+1)}{1-D} \rightarrow I_{in\_ave} = \frac{3(D+1)}{1-D}.I_{o\_ave} \quad (15)$$

$$I_{in\_ave} = \frac{3(D+1)}{1-D}.\frac{V_o}{R} = \frac{9(D+1)^2}{R(1-D)^2}.V_{in} \quad (16)$$

In the first interval that the switch is on, the relationship between the input current (I_{in}), the inductors (I_{L3}, I_{L2}, I_{L1}) and capacitive current (I_c) is:

$$I_{in} = I_{L1} + I_{L2} + I_{L3} - I_c + I_{c1} \quad (17)$$

And in the interval that the switch is off, the relationship between the input current (I_{in}), the inductors (I_{L3}, I_{L2}, I_{L1}) and capacitive current (I_c) is:

$$I_{in} = I_{L1} = I_{L2} = I_{L3} = I_c = I_{c1} = I_{c2} \quad (18)$$

Currents in both inductor and capacitor in the switching period are shown in Figure (8). the current in the inductor is:

$$I_L(t) = I_{L\min} + \frac{t}{L}V_{in} \quad (19)$$

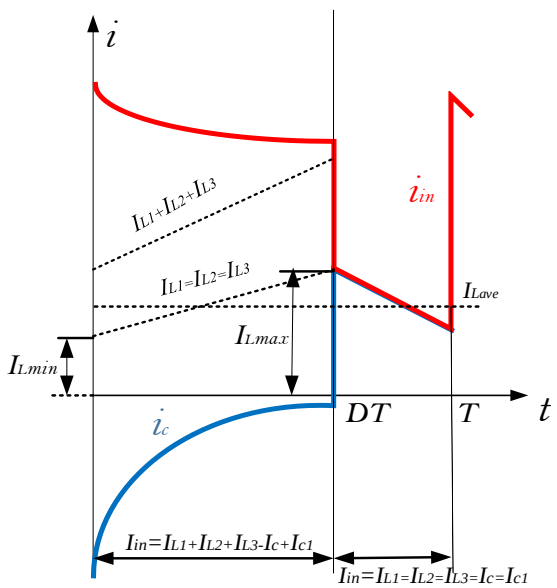

Figure 8. current in both inductor and capacitor switching

Now the average value of the input current and the capacitor current during the whole period is obtained by using the equation (19) as follows:

$$I_{n\_ave.off} = I_{c\_ave.off} = \frac{I_{L\min} + I_{L\max}}{2} = I_{L\min} + \frac{DT}{2L}V_{in} \quad (20)$$

$$I_{in\_ave.on} = I_{in\_ave.off} = I_{L\min} + \frac{DT}{2L}V_{in} \quad (21)$$

According to the current-second balance in capacitor C:

$$\frac{1}{T_s}\left(\int_0^{dT_s} I_{c\_on}dt + \int_{dT_s}^{T_s} I_{c\_off}dt\right) = 0 \quad (22)$$

$$I_{c\_ave.on} = I_{c\_ave.off} = \frac{-(1-D)}{D} \quad (23)$$

Using the equations (17) and (18) the relationship between average input current is rewritten:

$$I_{in\_ave} = I_{in\_ave.on}.DT + I_{in\_ave.on}.(1-D)T =$$
$$(3I_{L\_ave.on} - I_c + I_{c1}).DT + I_{in\_ave.off}.(1-D)T =$$
$$(3I_{L\min} + \frac{3DT}{2L}V_{in}).DT + (I_{L\min} + \frac{DT}{2L}V_{in}).(1-D)T = \quad (24)$$
$$2I_{L\min}(1+D) + (2D+1)\frac{DT}{2L}V_{in}$$

Comparing the equations (16) and (24) and setting I_L.min to zero the boundary condition between CCM and DCM is achieved:

$$\frac{9(D+1)^2}{R(1-D)^2}.V_{in} = 2I_{L\min}(1+D) + (2D+1)\frac{DT}{2L}V_{in}$$
$$\xrightarrow{I_{L\min}=0} R = \frac{18(D+1)^2 Lf}{D(2D+1)(1-D)^2} \quad (25)$$

Voltage ripple of capacitor C according to the average current value during the switch off interval is :

$$I_{c\_ave.off} = I_{L\min} + \frac{DT}{2L}V_{in} = \frac{I_{out}}{1-D}$$
$$\Delta V_c = \frac{I_{out}}{f\,c} = \frac{3(D+1)}{(1-D)R.f\,c}V_{in} \quad (26)$$

- Voltage ripple of output voltage during switch on interval by assuming constant discharge of the output capacitor C_o is:

$$\Delta V_{out} = \Delta V_{co} = \frac{D.I_{out}}{f\,c_o} = \frac{3D(D+1)}{(1-D)R.f\,c_o}V_{in} \quad (27)$$

The output voltage ripple and capacitor voltage ripple is shown in Figure 9. the figure shows that the output voltage ripple is much lower than the capacitor voltage ripple that is an advantage of the converter.

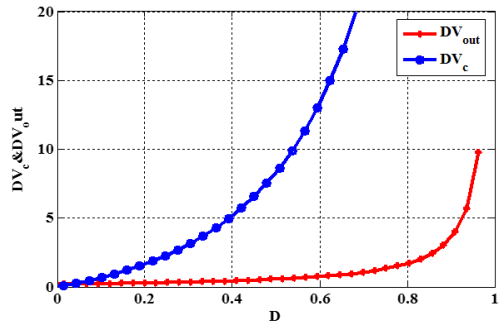

Figure 9. Curves of ripples for output voltage and capacitor C

7- Comparison Between Recent Topologies

In this section, the results of the comparative evaluation of the proposed converter and other interleaved high step-up converter proposed in [15], [16] and [17] based on voltage gain, the voltage stress on semiconductors devices and the number of magnetic cores are presented. Table I shows the performance comparison of some famous interleaved boost topologies.

According to the table, the proposed circuit makes the highest gain among other circuits. In addition, it is important to note that the lowest voltage stress among other topologies is obtained in the proposed circuit. It is pertinent to mention that this comparison clearly presents the superiority of the proposed method over other methods as discussed. This will make the proposed topology an excellent candidate for applications, such as PV, FCBC,HVDC and STATCOM that high voltage levels are required[18-21].

Table 1. PERFORMANCE COMPARISON AMONG INTERLEAVED HIGH STEP-UP CONVERTERS

High Step-Up Interleaved Converters	[16]	[17]	[15]	Proposed Converter
Voltage Gain	$\frac{1+D}{1-D}$	$\frac{1}{(1-D)^3}$	$\frac{3}{1-D}$	$\frac{3(D+1)}{1-D}$
Voltage stress on Switches	$\frac{V_o}{1+D}$	V_o	$\frac{V_o}{3}$	$\frac{1+2D}{3(D+1)}V_o$
Number of capacitors	4	3	5	4

8- Simulation Results

To evaluate the performance of the proposed converter, simulation is done with ORCAD software that considers parasitic elements as well as exact component models. The system parameters are as follows:

Vin= 20 V; fsw= 40 kHz; L1= L2= 0.4mH ; C = 80 mF; C1 = 45 mF; C2 = 1.5 mF; Co= 2.7 mF; R = 100Ω; D = 0.6

Power switch IRF250PCS and diodes BYQ28E-200 are also used in the converter. According to (12) the voltage gain of the converter is 12 and thus Vo = 240V. The simulated output voltage is equal to Vo = 230V in accordance with Fig. 10-a. the difference between theory and simulation results occur due to the parasitic elements that are not considered in the theory analysis. According to equations (6) - (8) capacitor voltage values should be VCo1 = 110V and VCo2 = 130V. However, the simulation results of capacitor voltages shown in Fig. 10-b present VCo1 = 105V and Vco2=120V. The simulation results of important circuit waveforms such as switch voltage, input current and capacitor current C and inductor currents are shown in Fig. 11-a, 11-b, 11-c, and 11-d. The converter efficiency is found to be 96.4% by simulation.

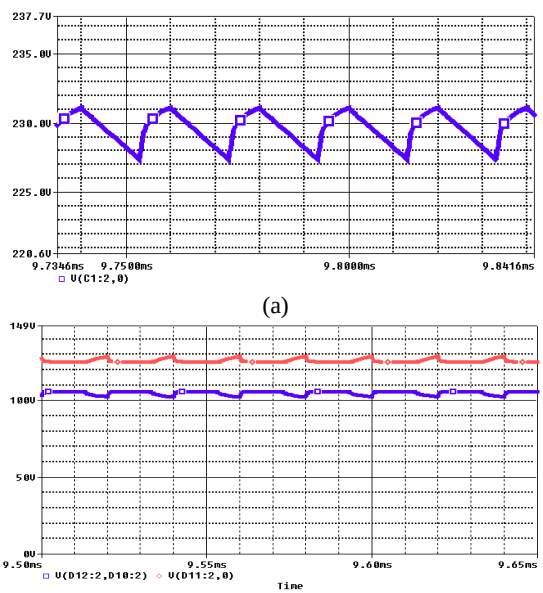

Figure 10. a) the output voltage. b) voltage capacitors VCo1 and VCo2

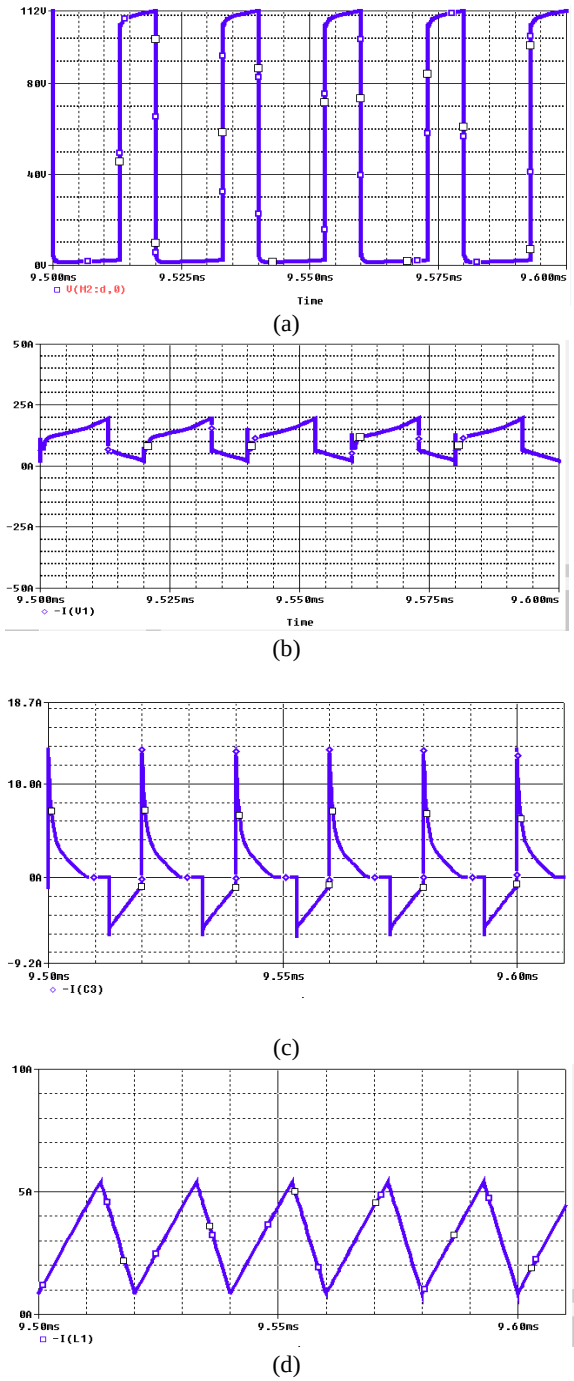

Figure 11. a) the voltage across the switch. b) input current. c) current across the capacitor C. d) The two ends of each of the inductors

9- Conclusions

In this paper, a new step-up DC-DC converter is proposed for renewable energy systems such as PV systems. The proposed converter can have high output gain that is crucial in the applications to prepare required output voltage levels from low voltage input obtained from PV panels. The converter is analyzed in both CCM and DCM. Finally, simulation with Orcad/Spice is done to verify the performance of the converter. The converter could successfully follow its designed values and the results show that it can work properly with its determined values. In comparison with other converters, this topology generates higher voltage gains.

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